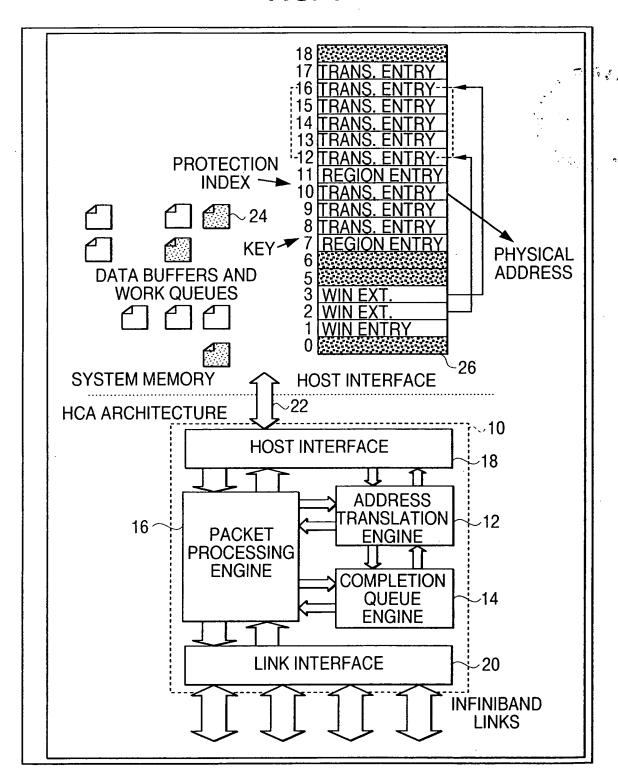
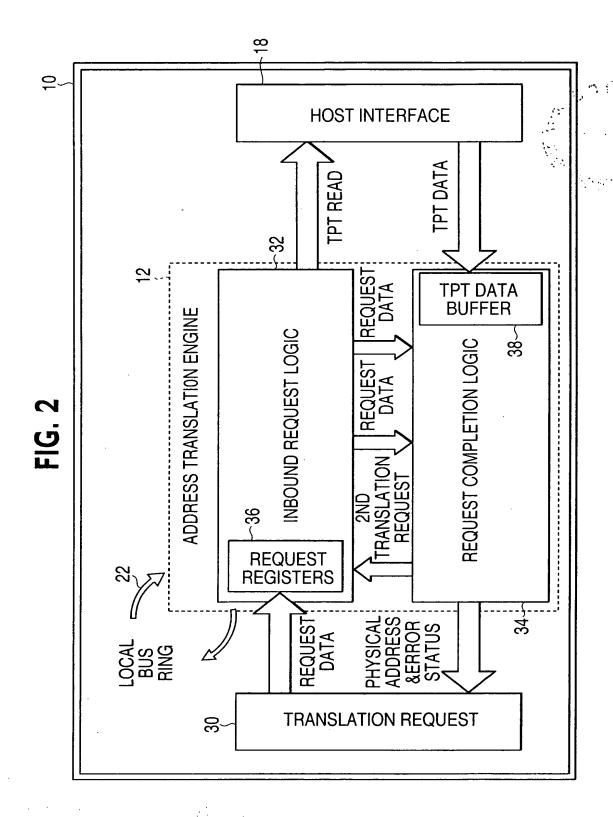
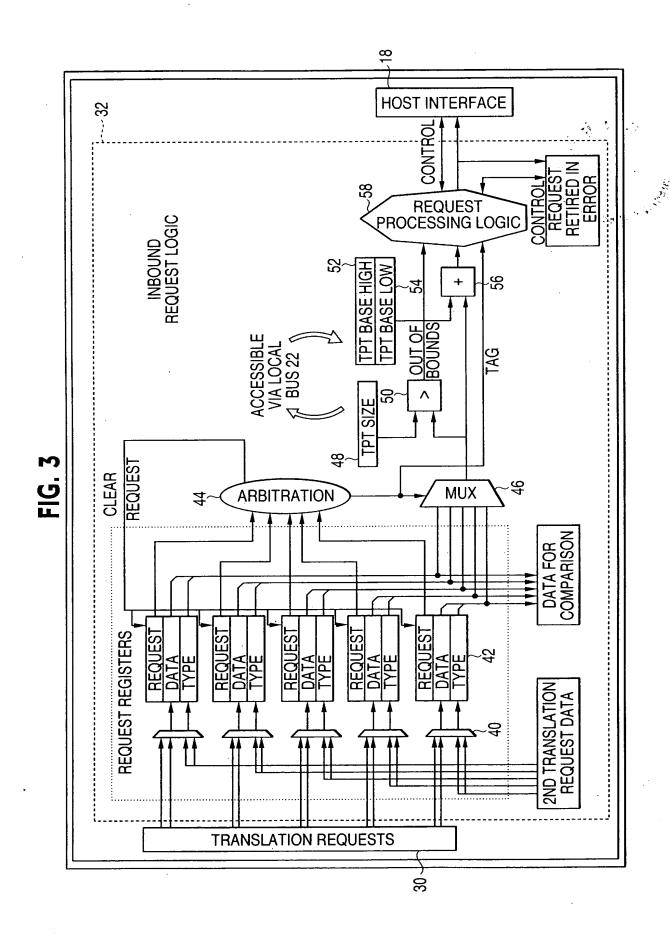
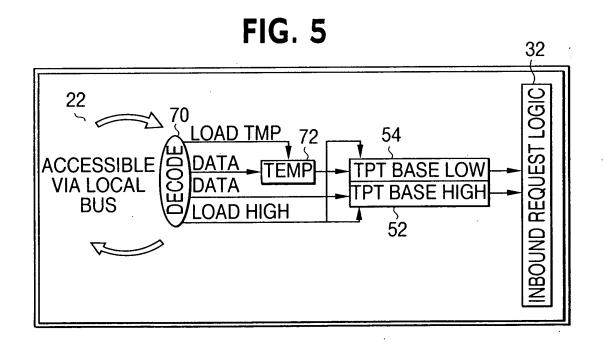
FIG. 1









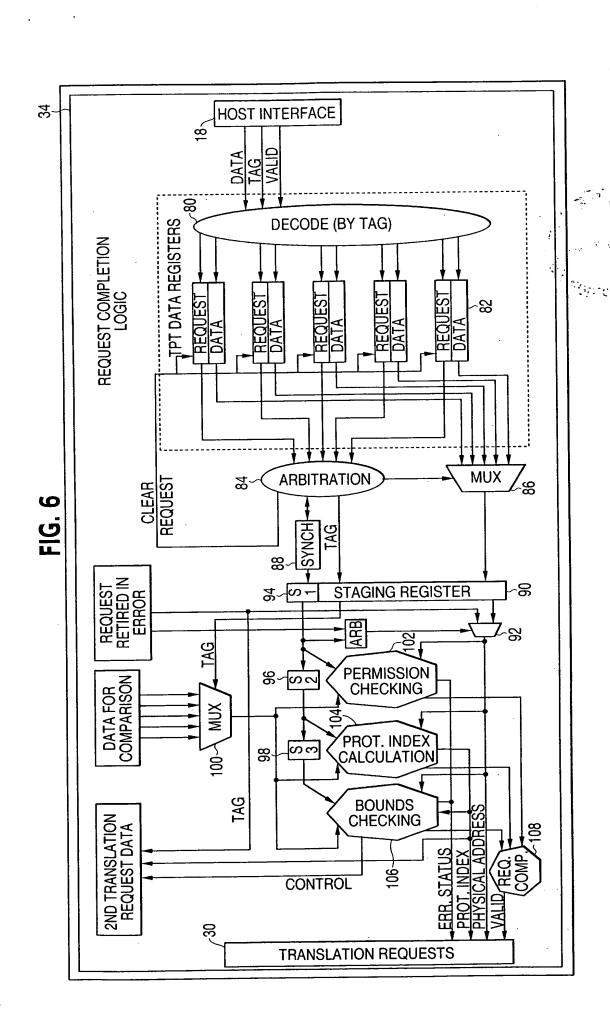


FIG. 7 120 DATA BUFFERS AND **WORK QUEUES COMPLETION EVENT QUEUES QUEUE** HOST INTERFACE SYSTEM MEMORY HCA ARCHITECTURE **~22** ~10 18~ **HOST INTERFACE PACKET COMPLETION** QUEUE ENGINE **PROCESSING ENGINE** 16 LINK INTERFACE ^20 **INFINIBAND LINKS** 

9 <del>,</del> 50 PACKET PROCESSING ENGINE <u>∞</u> HOST INTERFACE LINK INTERFACE DONE/ERROR STATUS CQ/EQ REQUESTS INBOUND WRITE REQUESTS PORT EVENTS 132 COMPLETION QUEUE ENGINE FINITE STATE MACHINE ADDRESS TRANSLATIONS ADDRESS TRANSLATIONS 136ر <u>~138</u> CQ WORK REGISTERS EQ WORK REGISTERS CQ CONTEXT MEMORY LOCAL BUS REGISTERS 130 134 ~23 LOCAL BUS RING

FIG. 8

FIG. 9

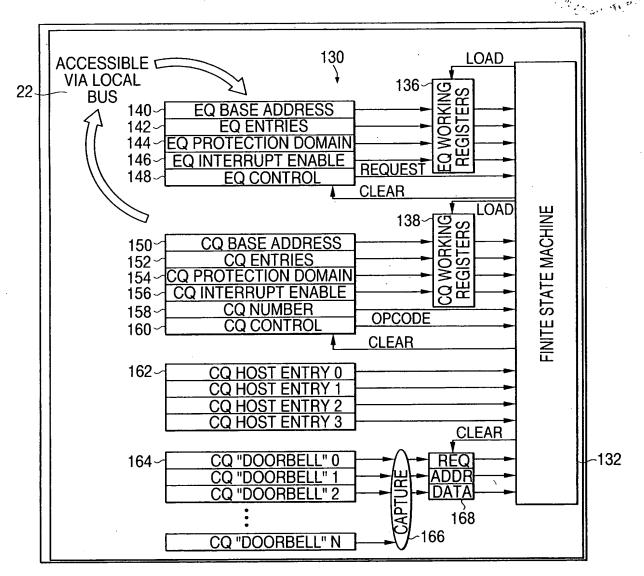


FIG. 10

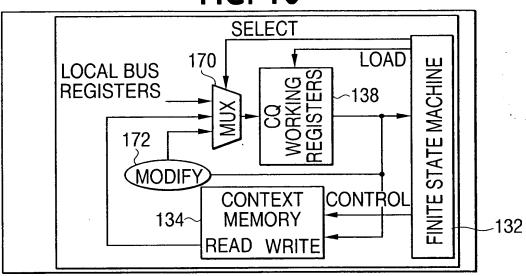


FIG. 11

,31 22,	21,20	13,12	0, 164
	1 COMP QUEUE	LETION NUMBER	104

FIG. 12

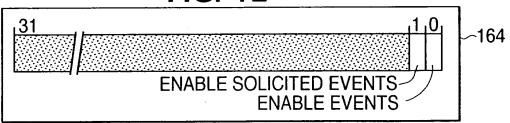


FIG. 13

